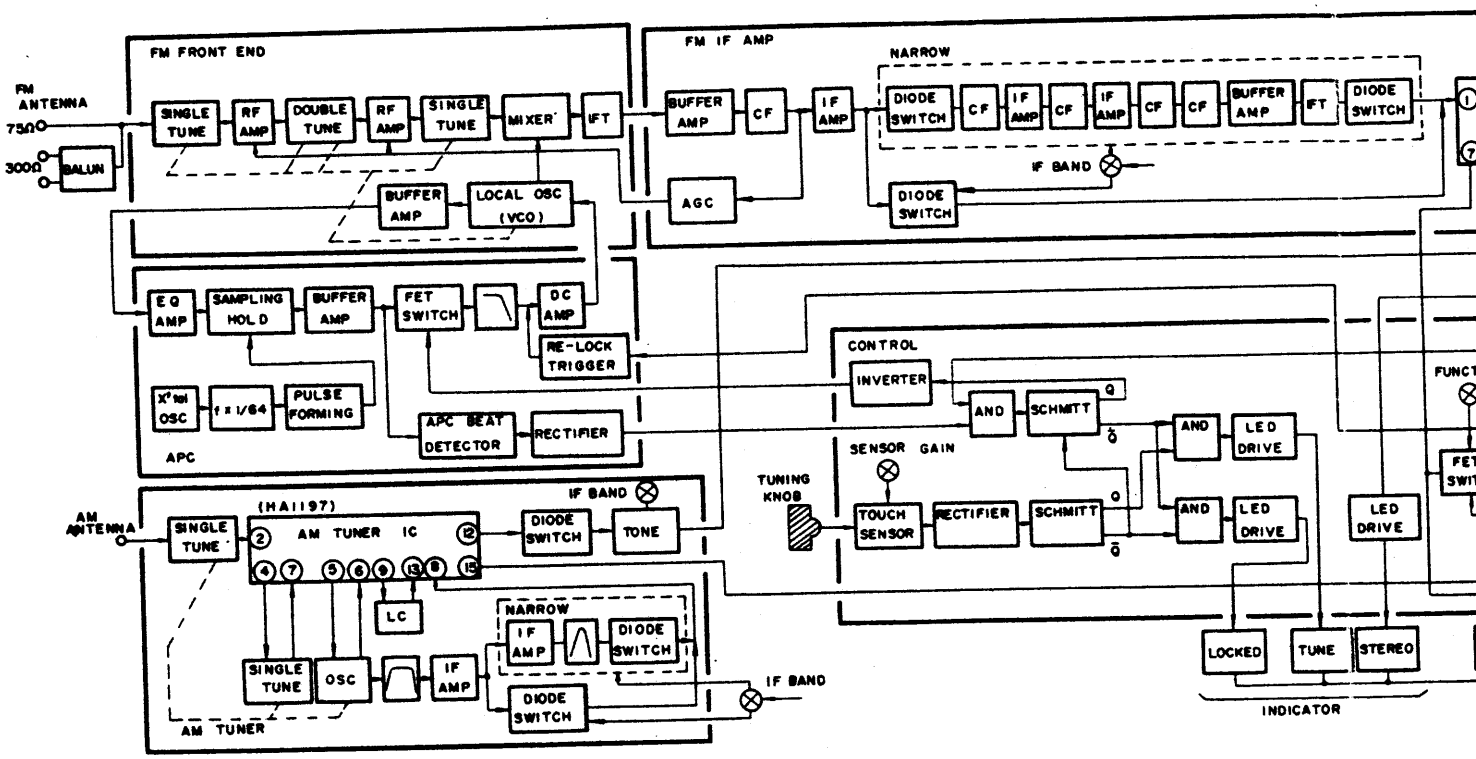
3. BLOCK DIAGRAM



4. CIRCUIT DESCRIPTIONS

4.1 SIGNAL CIRCUIT

FM Front-end

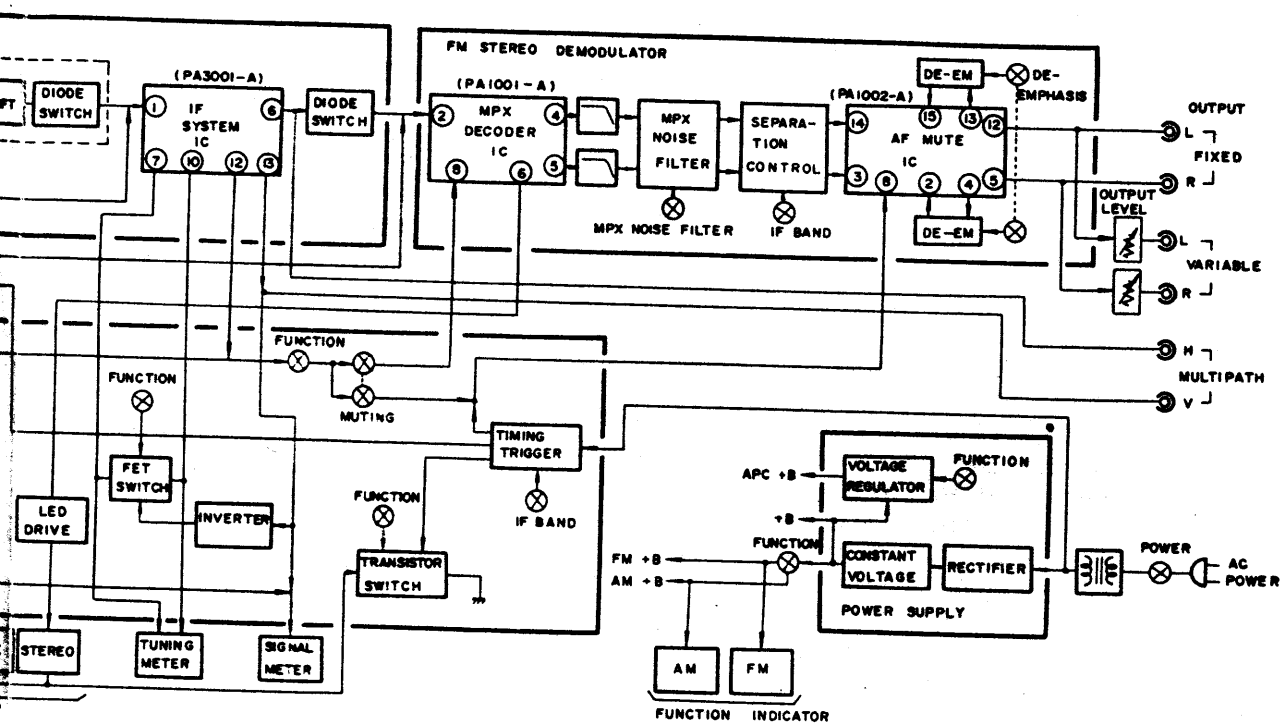
The FM front-end of this set uses a precision frequency-linear type 5-ganged tuning capacitor. The circuit is shown in Fig. 4-1. The antenna input is made an unbalanced (75Ω) by an M-coupled single-tuned circuit. The RF stage uses two dual-gate MOS FETs (Q_1, Q_2) having superior high-frequency characteristics. The interstage tuning circuits are C-coupled double-tuned for improved reception. The phase characteristic, spurious interference ratio, and IF interference ratio are especially good. A dual-gate MOS FET (Q_3) is also used at the mixer stage. The received signal is applied to gate 1 and the local oscillator signal is input at gate 2. The converted output (10.7MHz) is taken from the drain and applied to the IF amplifier thru an IFT. The local oscillator (Q_4) is modified Clapp circuit. Its output is fed to the mixer.

D_1 of the local oscillator is a vari-cap diode that forms part of the tuning capacitance. A vari-cap diode is an element whose capacitance can be controlled by means of the impressed voltage, and is designed to control the voltage relative to local oscillator frequency deviation to within ±100kHz. This control voltage is obtained from an APC (Automatic Phase Control) circuit. (See the description of the APC circuit on page 7.)

IF Amplifier

This tuner employs a dual IF amplifier consisting of a wide band IF amplifier designed for high separation, low distortion reproduction, and a narrow band IF amplifier used for rejection of interference signals (Fig. 4-2).

The wide band IF amplifier has been designed with the minimum number of frequency selective elements, with emphasis being placed on linear phase characteristics. The narrow band IF amplifier on the other band, has been designed with emphasis on selectivity. When the selector switch is in the wide position, the signal path is FM front-end → Q_8 → F_1 → Q_9 → T_2 → D_5, D_6 → PA3001-A, while in the narrow position it is FM front-end → Q_8 → F_1 → Q_9 → T_2 → D_4 → narrow IF amp. D_7 → PA3001-A. The changeover between wide and narrow is performed of diode switches (D_4 to D_7). When the selector switch is in the wide position, D_5 and D_6 are biased in the forward direction and D_4 and D_7 are biased in the reverse direction, thus bypassing the narrow IF amplifier. When the selector switch is in the narrow position, D_4 and D_7 are forward biased and D_5 and D_6 are reverse biased.



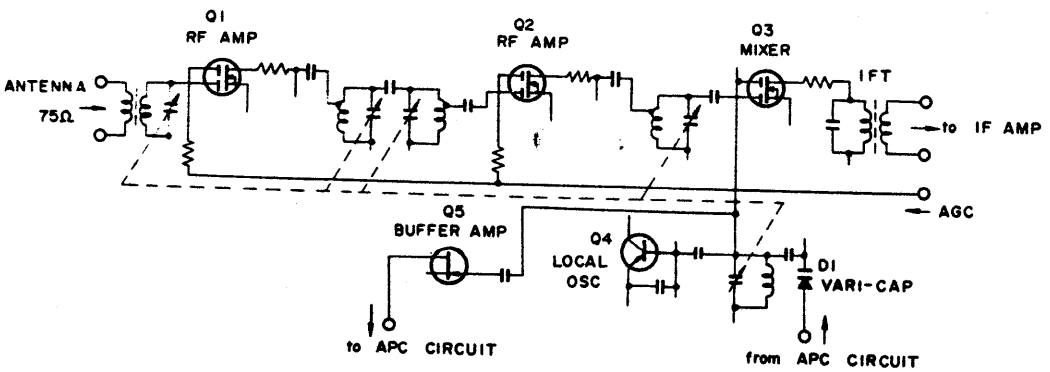


Fig. 4-1 FM front-end

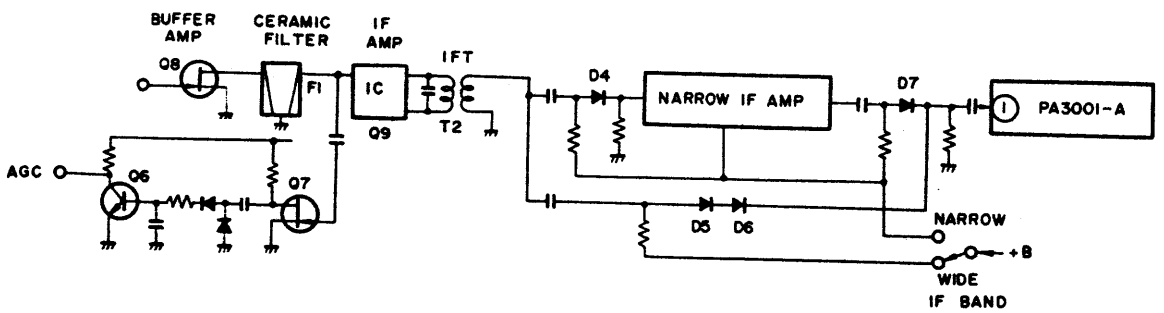


Fig. 4-2 FM IF amplifier

Multiplex Decoder

An IC (PA1001-A) developed by Pioneer is used in the stereo demodulation circuit. PA1001-A contains a PLL system VCO (Voltage Controlled Oscillator), NFB demodulator, automatic pilot conceller, and stereo/mono automatic switch. The NFB demodulator and automatic pilot canceller are special features of this IC. The NFB demodulator suppresses distortion caused by the non-linearity of the demodulation circuit. The automatic pilot canceller cancels the pilot signal (19kHz) in the stereo demodulation signal. This circuit cancels the pilot signal (19kHz) in the stereo demodulated signal by applying the 19kHz from the VCO synchronized with the pilot signal (19kHz) in the composite signal to the stereo demodulated signal thru an AGC amp. Moreover, since the cancel signal level tracks the input pilot signal level by means of the AGC amp., the rejection ratio remains the same even with changes in input pilot signal level.

Output Amplifier

An AF MUTE IC (PA1002-A) is employed in the final stage of the tuner. This IC contains two AF amplifiers for L and R channels, together with a muting gate circuit. These AF amplifiers employ time constant NFB to provide de-emphasis characteristics. The muting gate circuit is electrically connected to the signal circuit when a DC voltage is applied to pin no.8 of the PA1002-A (Refer to muting control in page 10).

4.2 APC CIRCUIT

The APC circuit stablizes the receiving state by suppressing changes in the FM front-end local oscillator frequency.

This circuit is a PLL circuit that controls the frequency of the local oscillator (VCO; Voltage Controlled Oscillator) by comparing the phase of a reference frequency produced by a crystal oscillator and the phase of the local oscillator frequency, and then using the DC voltage corresponding to their phase difference to control the local oscillator. The capture range (range over which circuit is locked) of this APC is approximately ±12kHz, and its lock range (range which can be controlled by APC) is ±75kHz. Fig. 4-3 is the block diagram of this circuit.

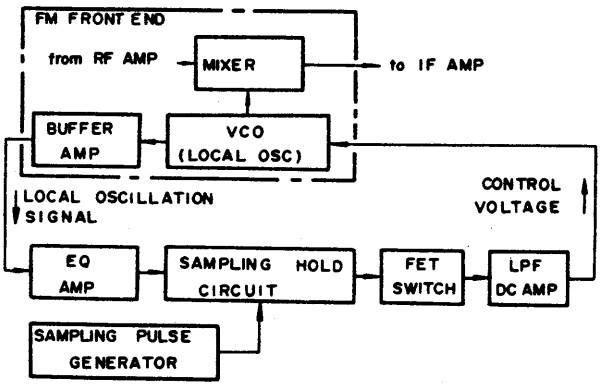


Fig. 4-3 Block diagram of APC circuit

Sampling Pulse Generator

This circuit uses 3 digital ICs and one crystal (Fig. 4-4). The crystal and two NAND gates on M5S003P from an oscillator circuit that oscillates at the reference frequency (6.4MHz).

This reference frequency is converted to a 100kHz square wave by dividing it by four with M53273P and then dividing it by sixteen with M53293P. This 100kHz square wave is applied to two NAND gates on M5S003P and shaped to a 100kHz sampling pulse (Fig. 4-5). This sampling pulse is then applied to the sampling hold circuit.

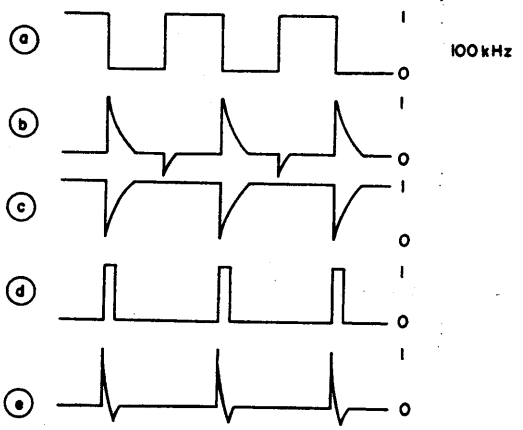


Fig. 4-4

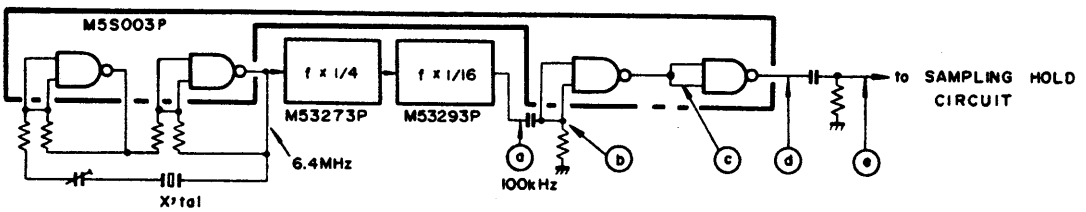


Fig. 4-5 Sampling pulse generator

Sampling Hold Circuit

The sampling hold circuit compares the phases of the local oscillation frequency and sampling pulse, and generates a voltage corresponding to their phase difference (Fig. 4-6). When the sampling pulse is applied to the base of Q_3, Q_3 is turned on, and current flows thru Q_2. When the pulse is removed, Q_3 is turned off, and a flyback pulse is generated at the base of Q_2 at this instant by the inductance component of the circuit. C_5 is charged by this flyback pulse and Q_2 is then turned off. When the next sampling pulse is applied, the charge across C_5 is discharged thru Q_3 and C_5 is recharged by the flyback pulse generated at the base of Q_3 at this time. The voltage waveforms of each part are shown in Fig. 4-7. This becomes as shown in Fig. 4-8 when the local oscillation frequency is applied to the base of Q_2.

Fig. 4-8a is the waveform when the sampling pulse and local oscillation frequency are in phase, and Fig. 4-8b is the composite waveform when there is a phase difference. Therefore, a voltage corresponding to the phase difference between the sampling pulse and local oscillation frequency is hold. The C_5 hold voltage waveform is shown in Fig. 4-9.

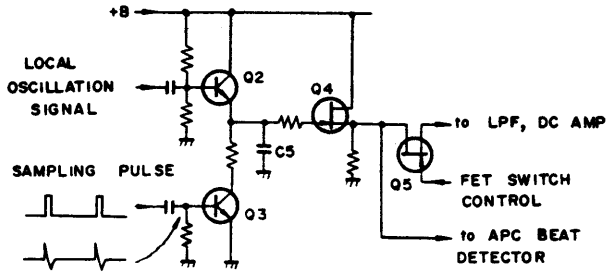


Fig. 4-6 Sampling hold circuit

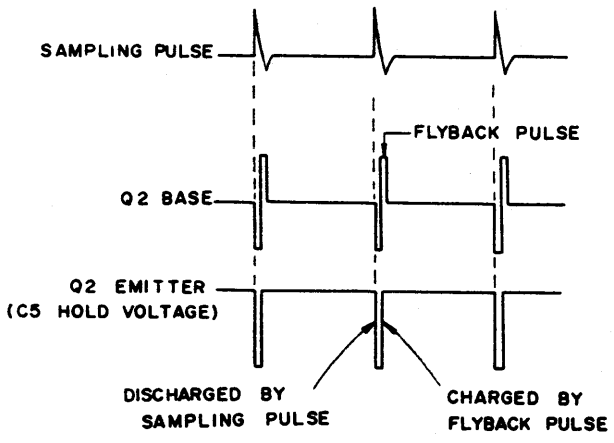


Fig. 4-7 Voltage waveforms

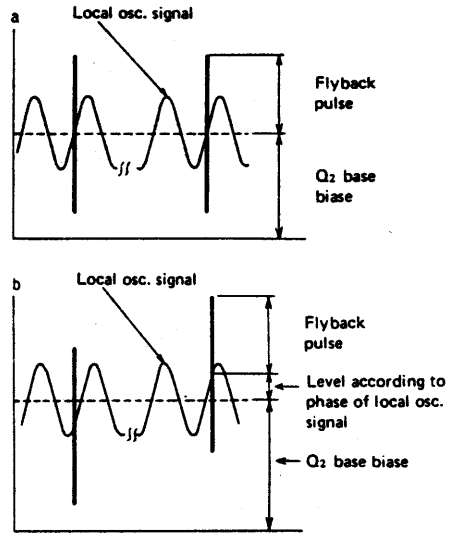


Fig. 4-8 Q2 base waveforms

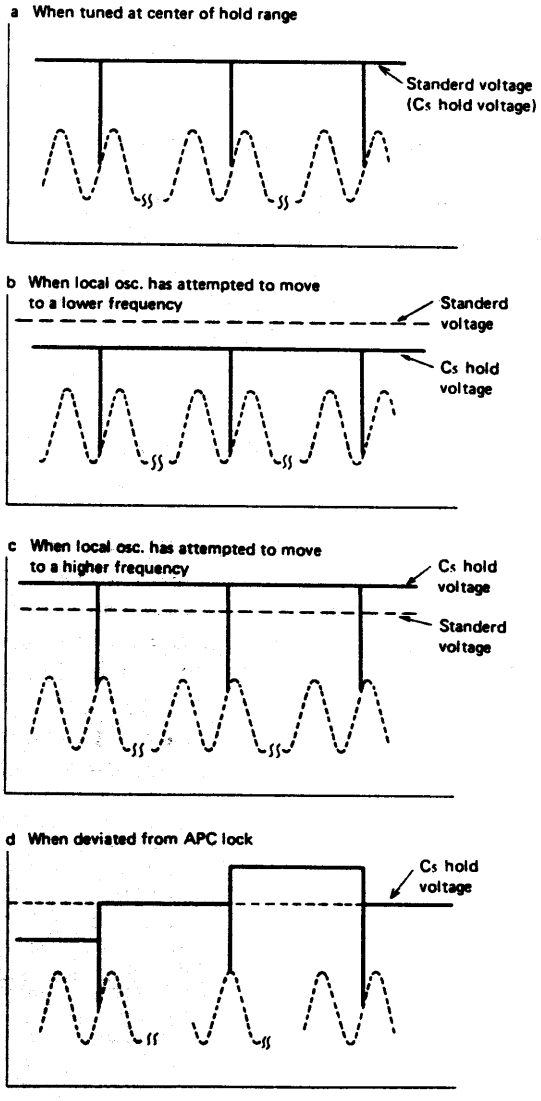


Fig. 4-9 Cs hold voltage waveforms

4.2 CONTROL CIRCUIT

NOTE:
The control circuit is operated digitally. Consequently, voltage changes are represented by "H" (high level voltage) and "L" (low level voltage) in the description.

APC Operation Control

The FET switch (Q_5) in the APC circuit is turned off when the tuning knob is touched. During this time, a reference voltage (+8V) is applied to the variable capacitance diode in the FM front-end local oscillator to permit station tuning operations with the APC turned off.

When an input signal whose antenna input level is at least 20dBf (5.5μV) is tuned, the TUNE indicator LED is turned on. And when the tuning knob is then released, the FET switch (Q_5) is turned on, thereby completing the APC circuit loop to "lock" the local oscillator frequency. The TUNE indicator LED subsequently turns off, and the LOCKED indicator LED turns on instead. These operations are all controlled by the touch sensor, APC beat detector, and the output from pin no.12 of the IF system IC (PA3001-A). (See Fig. 4-10).

When the tuning knob is touched by hand, noise voltage induced by the human body is detected and amplified by the touch sensor. The sensor output is then rectified and employed as the Schmitt A control voltage. When an APC beat signal of at least 7kHz appears at the output of the sampling hold circuit, it is detected, and then amplified by the APC beat detector. (APC beat signals are generated at the sampling hold circuit output if the FM front-end local oscillator fails to remain at an integer multiple of 100kHz. The frequency of this beat signal lies within the DC~50kHz range, and is determined by the phase difference between the sampling pulse and the oscillator frequency). The output of the APC beat detector is rectified, and employed as the Schmitt B control voltage. When a station is tuned away by more than ±65kHz, or if the antenna input level is below 20dBf, a DC voltage appears at pin no.12 of the IF system IC (PA3001-A), this also being used to control Schmitt B.

Consequently, when the antenna input level of the tuned signal exceeds 20dBf, the collector voltage of Q_{32} in Schmitt A will be set to "L", and the collector voltage of Q_{33} set to "H". And with the collector voltage of Q_{38} in Schmitt B at "H", the collector voltage of Q_{37} is also set to "H" (by the Q_{32} collector voltage). The base voltage of Q_{35} is thereby increased, resulting in this transistor being turned on to light up the TUNE indicator. Since Q_{34} remains off because of a low base voltage, the LOCKED indicator does not light up at this time. And since Q_{36} has already been turned on by the collector voltage of Q_{37}, the gate voltage of the APC circuit FET switch (Q_5) will be low, which means this switch will also remain off.

When the tuning knob is then released, the collector voltages of Schmitt A Q_{32} and Q_{33}, and Schmitt B Q_{37} will all be inverted, resulting in Q_{35} (TUNE indicator LED) being turned off, and Q_{34} (LOCKED indicator LED) being turned on. Q_{36} is also turned off to turn the FET switch (Q_5) on.

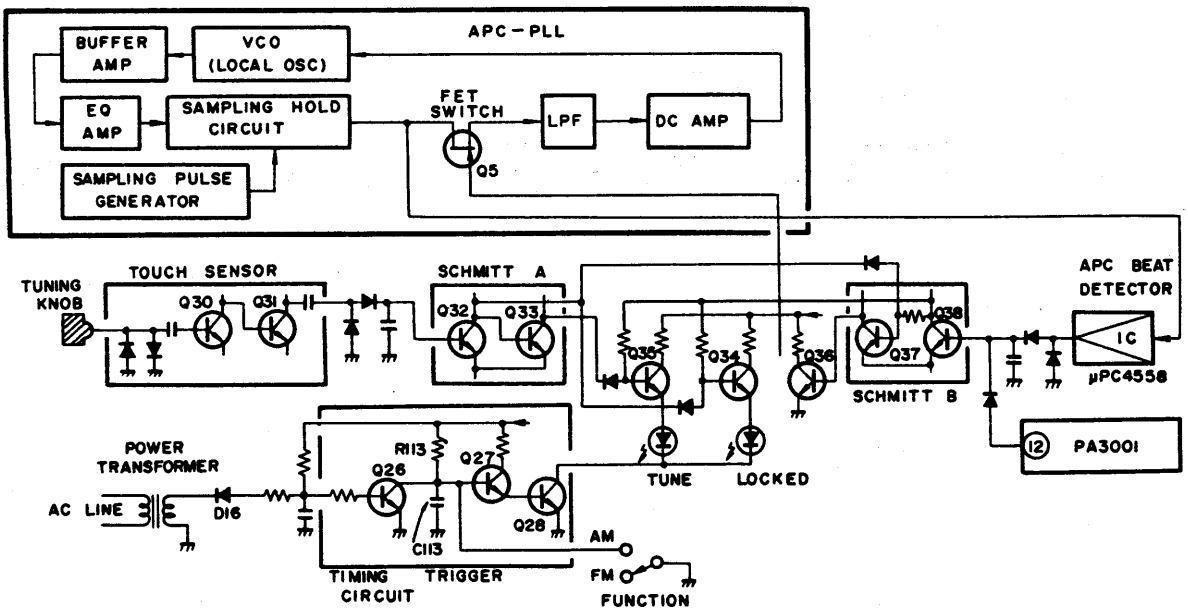


Fig. 4-10 APC operation control circuit

Timing Trigger Circuit

This circuit is designed to delay the lighting up of the indicator LEDs (TUNE, LOCKED, STEREO) when the power is switched on, and to turn them off immediately when the power is switched off again. (See Fig. 4-10).

When the power is switched on, Q_{26} is turned off immediately by a negative voltage applied via D_{16}. The base voltage of Q_{27} is thereby increased gradually, the increase being controlled by the R_{113}/C_{113} time constant. Once the voltage reaches +1.2V (approx.), Q_{27} and Q_{28} are both turned on, thereby turning on all relevant indicator LEDs.

When the power is switched off again, the negative voltage applied via D_{16} is cut immediately, resulting in Q_{26} being turned on. C_{113} therefore discharges directly via Q_{26} to turn Q_{27} and Q_{28} off. All indicator LEDs will consequently turn off immediately. This same result is also achieved when the FUNCTION selector is in the AM position. This is due to the fact that the base of Q_{27} is connected to ground by the FUNCTION selector, thereby turning Q_{27} and Q_{28} off.

Re-lock Trigger Circuit

When the power is switched on, this re-lock trigger circuit activates a sweep of the local oscillator frequency, covering a range of up to 100kHz both sides of the frequency indicated by the dial pointer at the time. If a signal of antenna input level in excess of 20dBf is detected in this range, the frequency is automatically re-locked by the APC circuit. (See Fig. 4-11).

In this case, when the power is switched on Q_{23} is turned off immediately by the negative voltage applied via D_{16}, resulting in the voltage changes at different places describing different curves as shown in Fig. 4-12. The voltage applied to the variable capacitance diode in the local oscillator is represented by curve (e), thereby causing the local oscillator frequency to change, or "sweep" within a limited range. If an input signal whose antenna input level exceeds 20dBf is detected during this sweep, the APC circuit FET switch is turned on, resulting in the frequency of that input signal being locked by the APC circuit.

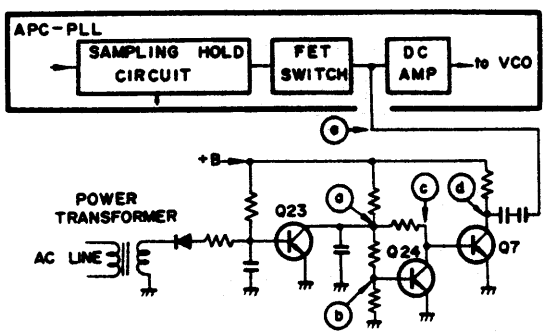


Fig. 4-11 Re-lock trigger circuit

Muting Control Circuits

This tuner features 3 major muting actions.

(1) Inter-station muting in the FM band and muting of weak FM stations.
(2) Muting of switching noises when FUNCTION selector and IF BAND switch are operated.
(3) Muting when POWER switch is turned on and off.

All muting action is controlled by the muting gate included in the AF MUTE IC (PA1002-A). (See Fig. 4-13).

(1) Inter-station Muting in FM Band

When any FM input signal whose antenna input level is below 20dBf (5.5μV) is received (which also covers the case when no input signal is received), a DC voltage appears at pin no.12 of the IF system IC (PA3001-A). If the MUTING switch has been turned on, this DC voltage is applied to pin no.8 of the AF MUTE IC (PA1002-A) to activate the muting circuit.

(2) Muting of Switching Noises (FUNCTION Selector and IF BAND Switch)

When either the FUNCTION selector or the IF BAND switch is switched to another position, the Q_{29} base potential is dropped momentarily, resulting in Q_{29} being turned on during the same brief moment. During this interval, C_{114} is charged up, the charge then being applied to pin no.8 of PA1002-A. The muting time is thus determined by the C_{114}/R_{115} time constant.

(3) Power Switch Muting

The muting trigger employed when the POWER

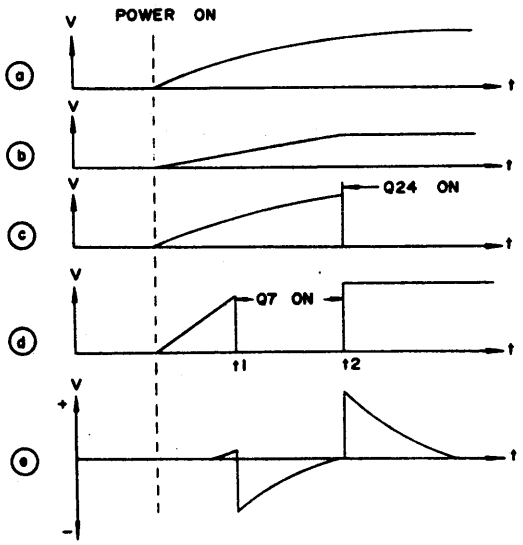


Fig. 4-12 Voltage waveforms

switch is turned on and off is formed by Q_{23} and Q_{25}. When the POWER switch is turned on, Q_{23} is turned off by the negative voltage applied via D_{16}. The consequent voltage changes at points (a) and (b) are shown in Fig. 4-14. The point (b) voltage is applied to pin no.8 of PA1002-A. When the POWER switch is turned off, Q_{23} is turned on due to the immediate cut off of the negative voltage applied via D_{16}. Q_{25} is then turned off as a result of the voltage at point (a) dropping to 0V, thereby generating a muting trigger action at point (b).

4.4 AM TUNER

The AM tuner stage is equipped with a 3-ganged tuning capacitor and an IC (HA1197). The IF amplifier stage includes a "wide IF amplifier" stage (for improved quality of sound) and a "narrow IF amplifier" stage (for better selectivity). (See Fig. 4-15).

The WIDE and NARROW positions are switched by switching the bias of D_{14} and D_{15}, thereby altering the signal path. In the NARROW position, D_{15} is turned on, resulting in the inverse biasing of D_{14}, and the IF signal being passed via F_9 (narrow band-pass filter). In the WIDE position, the D_{15} bias is removed, resulting in D_{14} being biased in the forward direction, and the IF signal being bypassed via D_{14}.

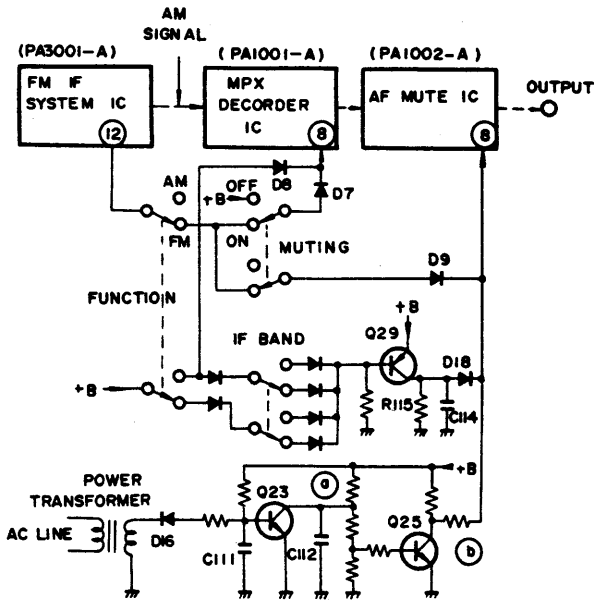


Fig. 4-13 Muting control circuit

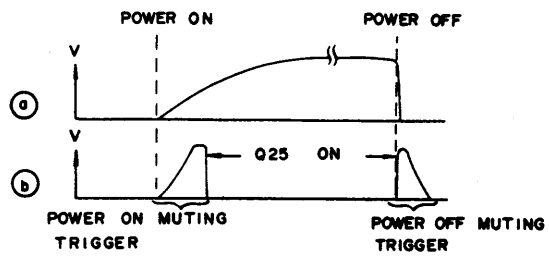


Fig. 4-14 Voltage waveforms

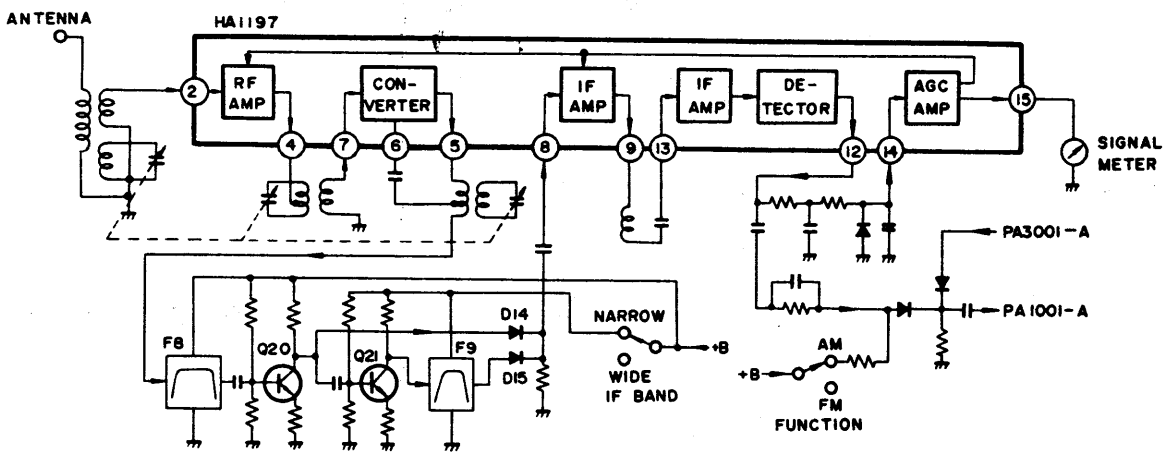


Fig. 4-15 AM tuner